Amendments to the Claims:

Listing of Claims:

1. (Currently amended) A method of fabricating integrated circuits having both high voltage and low voltage devices, wherein a provided substrate contains at least one high-voltage device area and at least one low-voltage device area, and a first pad oxide layer over the substrate, the method comprising:

performing a first ion implantation process to form a first ion well of a first conductivity type in the substrate within the high-voltage device area;

performing a second ion implantation process to form a second ion well of a second conductivity type in the substrate within the high-voltage device area;

stripping the first pad oxide layer;

forming a second pad oxide layer;

forming a masking layer over the second pad oxide layer;

forming a plurality of openings in the masking layer to exposed a portion of the second pad oxide layer;

performing a third ion implantation process to implant ions of the first conductivity type into the second ion well within the high-voltage device area, to form a first drift layer;

thereafter performing a fourth ion implantation process to implant ions of the first conductivity type into the low-voltage device area, to form a third ion well of the first conductivity type;

thereafter performing a fifth ion implantation process to implant ions of the second conductivity type into the low-voltage device area, to form a fourth ion well of the second conductivity type;

thereafter performing a sixth ion implantation process to implant ions of the second conductivity type into the first ion well within the high-voltage device area, to form a second drift layer;

performing an oxidation process to form a plurality of field oxide isolation structures through the openings in the masking layer;

removing the masking layer and the second pad oxide layer;

forming a first gate oxide layer over the substrate;

~~performing a seventh and eighth ion implantation processes to implant ions of the~~

~~first conductivity type into the second ion well and implant ions of the second conductivity type into the first ion well, thereby forming a first channel stop regions within the high-voltage device area;~~

performing a seventh ion implantation processes to implant ions of the first conductivity type into the first ion well to form a first channel stop region within the high-voltage device area;

performing an eighth ion implantation processes to implant ions of the second conductivity type into the second ion well to form a second channel stop region within the high-voltage device area;

~~performing a ninth ion implantation process to form a second channel stop region in the fourth ion well within the low-voltage device area;~~

performing a ninth ion implantation process in the fourth ion well within the low-voltage device area to form an anti-punch-through doping region in the fourth ion well;

forming an anti-punch-through doping region in the fourth ion well;

removing the first gate oxide layer within the low-voltage device area;

growing a second gate oxide layer within the low-voltage device area; and

~~formign~~ forming a plurality of gate structures on the first and second gate oxide layers.

2. (Original) The method of claim 1 wherein the first conductivity type is N type, and the second conductivity type is P type.

3. (Original) The method of claim 1 wherein the masking layer comprises silicon nitride layer.

4. (Original) The method of claim 1 wherein the first gate oxide layer has a thickness of about 700~900 angstroms.

5. (Original) The method of claim 1 wherein the second gate oxide layer has a thickness of about 50~70 angstroms.

6. (Original) A high-voltage semiconductor process compatible with low-voltage process, comprising:

preparing a substrate comprising at least one high-voltage device area and at least one low-voltage device area thereon;

implanting an N well and a P well into the high-voltage device area;

performing a first ion drive-in process to activate the N well and P well of the high-voltage device area;

forming a pad oxide layer and a masking layer over the substrate;

forming a plurality of openings in the masking layer to expose a portion of the pad oxide layer;

implanting N type dopants into the P well of the high-voltage device area to form a first drift layer;

performing a second ion drive-in process to activate the first drift layer;

implanting an N well and a P well into the low-voltage device area;

performing a third ion drive-in process to activate the N well and P well of the low-voltage device area;

implanting P type dopants into the N well of the high-voltage device area to form a second drift layer;

performing an oxidation process to form a plurality of isolation structures through the openings in the masking layer;

removing the masking layer;

implanting a plurality of grade regions in the high-voltage device area;

removing the pad oxide layer;

forming a first gate oxide layer on the substrate, and simultaneously driving in the plurality of grade regions in the high-voltage device area;

masking the high-voltage device area and removing the first gate oxide layer in the low-voltage device area;

growing a second gate oxide layer in the low-voltage device area; and

forming a plurality of gate structures in the low-voltage device area and the high-voltage device area.

7. (Original) The high-voltage semiconductor process compatible with low-voltage

process according to claim 6 wherein the masking layer is silicon nitride layer.

8. (Original) The high-voltage semiconductor process compatible with low-voltage process according to claim 6 wherein the isolation structures are field oxide layers.

9. (Original) The high-voltage semiconductor process compatible with low-voltage process according to claim 6 wherein the first gate oxide layer has a thickness of about 700~900 angstroms.

10. (Original) The high-voltage semiconductor process compatible with low-voltage process according to claim 6 wherein the second gate oxide layer has a thickness of about 50~70 angstroms.

11. (Original) The high-voltage semiconductor process compatible with low-voltage process according to claim 6 wherein after driving in the plurality of grade regions in the high-voltage device area and before removing the first gate oxide layer in the low-voltage device area, the high-voltage semiconductor process compatible with low-voltage process further comprising the steps of:

implanting N type ions into the N well of the high-voltage device area to form N type channel stop; and

implanting P type ions into the P well of the high-voltage device area to form P type channel stop.

12. (Original) The high-voltage semiconductor process compatible with low-voltage process according to claim 6 wherein after driving in the plurality of grade regions in the high-voltage device area and before removing the first gate oxide layer in the low-voltage device area, the high-voltage semiconductor process compatible with low-voltage process further comprising the step of:

implanting an N type anti-punch-through doping region into the P well of the low-voltage device area.